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EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/517,109	WAGNER ET AL.	
	Examiner	Art Unit	
	JOSEPH SCHELL	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-15 have been examined.

Claims 1-15 have been rejected.

Response to Arguments

1. The arguments submitted April 8, 2008 have been fully considered but are moot in view of the new grounds of rejection.

Claim Objections

2. Claim 10 line 1 should read "as claimed in claim 1 or at least".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112 second paragraph as being indefinite. Claim 4 line 4 states that the memory area "can be written to only after a reset". Unless a system is caught immediately after an unheard of live-construction where the memory is added while the system is already powered, all system interaction occurs after a reset. Therefore the limitation that the memory area can only be written to after a reset appears to be non-limiting and is indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki (US Patent 4,461,003) in view of Koch ('665).

5. As per claim 1, Tamaki ('003) discloses a method for at least one microcontroller unit that is intended for at least one application and is associated with a system wherein

- the microcontroller unit has at least one non-volatile memory area associated with it (as shown in Figure 1, element 504),

- the memory area can be read from and written to by the microcontroller unit (column 3 lines 5-11, a conventional microcomputer arrangement of processor-controlled non-volatile memory implies that it can be written to and read by the processor).

Tamaki ('003) does not expressly disclose the system for monitoring the operation of the microcontroller and wherein at least one set of statistics, including at least a set of fault statistics, relating to the operation of the microcontroller unit, can be kept by means of the memory area.

Koch ('665) teaches a motor vehicle system that contains two processors that error check each other and count reset events (column 2 lines 38-42 and column 4 lines 8-13).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the vehicle microcontroller of Tamaki ('003) such that it contains two processors and saves a count of reset signals as taught by Koch ('665). This modification would have been obvious because multiple processors allow for one processor to monitor the other (Koch ('665) column 1 line 65 through column 2 line 8) and the reset counting allows for processor failure to be detected and safely compensated for (Koch ('665) column 4 lines 23-29).

6. As per claim 2, Tamaki ('003) in view of Koch ('665) discloses a method as claimed in claim 1, wherein the memory area is permanently supplied by at least one battery unit (Tamaki ('003) column 3 lines 1-4).

7. As per claim 3, Tamaki ('003) in view of Koch ('665) discloses a method as claimed in claim 1 or 2, wherein

- in relation to the operation of the microcontroller unit a distinction can be made between different reset events (Koch ('665) column 4 lines 18-21), and

- these different reset events can be made accessible to the microcontroller

unit (Koch ('665) column 4 lines 18-21, the distinguishing of the warm and cold reset events would have been obvious because certain POST measures need only be taken on cold reset events, see Koch ('665) column 1 lines 28-33).

8. As per claim 4, Tamaki ('003) in view of Koch ('665) discloses the method as claimed in any of claims 1 to 2 wherein the memory area

-can be read from at any time (see Tamaki ('003) Figure 1, when the voltage detector 700 detects a low voltage is can only disable non-volatile RAM 504, memory area 502 is still accessible to the CPU) and

-can be written to only after a reset or while the system is restarting (Tamaki ('003) teaches that the vehicle battery is checked and nonvolatile memory read and write access is disabled when the voltage is low (see abstract)).

9. As per claim 5, this claim recites limitations found in claim 1 and is rejected on the same grounds as claim 1.

10. As per claim 6, Tamaki ('003) in view of Koch ('665) discloses the base chip as claimed in claim 5, including

-at least one information unit is provided to allow for different reset events (Koch ('665) column 4 lines 13-14, the reset counter),

-at least one reset unit for resetting the microcontroller unit, which reset unit is connected to the microcontroller unit (Koch ('665) column 4 lines 11-13, one processor resets the other), and

-at least one supply unit that is connected to the microcontroller unit (as shown in Figure 1 of Tamaki ('003), the voltage regulator 300).

11. As per claim 7, Tamaki ('003) in view of Koch ('665) discloses a base chip as claimed in claim 6, wherein

- the memory area and the supply unit are permanently supplied with power from at least one battery unit (as shown in Tamaki ('003) Figure 1, and column 3 lines 1-4, the first voltage regulator 300 and the non-volatile RAM 504 are both powered by the battery 100)

- the microcontroller unit has at least one temporary energy supply provided to it via the supply unit (as shown in Tamaki ('003) Figure 1, the CPU is powered by the first voltage regulator).

12. As per claim 8, Tamaki ('003) in view of Koch ('665) discloses a base chip as claimed in any of claims 6 to 7, wherein the memory area and the information unit have inserted in front of them at least one interface unit for exchange of data with the microcontroller unit (Koch ('665) column 3 lines 61-66 and column 4 lines 13-14, the processor interfaces with the reset counter and the memory).

13. As per claim 9, Tamaki ('003) in view of Koch ('665) discloses a system including at least one microcontroller unit intended for at least one application and at least one base chip as claimed in any of claims 5 to 7 (Tamaki ('003), see abstract).

14. As per claim 10, Tamaki ('003) in view of Koch ('665) discloses use of a method as claimed in claim 1 or of at least one base chip as claimed in claim 5 for monitoring the operation of at least one microcontroller unit intended for at least one application in automobile electronics (Koch ('665) column 1 lines 6-8, column 1 lines 65-67, and column 3 line 64 through column 4 line 7).

15. As per claim 13, Tamaki ('003) in view of Koch ('665) discloses the base chip of claim 5, wherein the at least one non-volatile memory area comprises a random access memory (Tamaki ('003) column 3 line 62, it is a non-volatile RAM).

16. Claims 11-12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki ('003) in view of Koch ('665) and Anderson ('453).

17. As per claim 11, Tamaki ('003) in view of Koch ('665) discloses the method of claim 1. Tamaki ('003) in view of Koch ('665) also discloses the counting of warm reset events (Koch ('665) column 4 lines 21-29). Tamaki ('003) in view of Koch ('665) does not expressly disclose the counting of different types of reset events.

Anderson ('453) teaches counting of power failure events (column 2 lines 6-25).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Tamaki ('003) in view of Koch ('665) such that it counts power failure events in addition to warm resets. This modification would have been obvious because it allows the system to preserve data that may have been corrupted if a power failure occurred while data was being accessed (Anderson ('453) column 1 lines 60-63 and column 2 lines 50-63).

18. As per claim 12, Tamaki ('003) in view of Koch ('665) and Anderson ('453) discloses the method of claim 11, further comprising:

comparing a number of at least one type of reset event to a threshold (Koch ('665) Figure 3); and

when the number of the at least one type of reset event is greater than the threshold, operating the microcontroller unit in a low-energy mode (Koch ('665) column 1 lines 60-64).

19. As per claims 14-15, these claims recite limitations found in claims 11-12 and are rejected on the same grounds as claims 11-12.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH SCHELL whose telephone number is (571)272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

JS